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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,588	08/18/2003	Kitrick Sheets	1376.720US1	4010

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EXAMINER	
TSAI, SHENG JEN	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,588	SHEETS, KITRICK	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *2,3,7,8,12 and 13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6,9-11 and 14-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicant's Amendment and Remarks filed on February 28, 2006 regarding application 10,643,588 filed on August 18, 2003.

2. Claims 1, 4, 6, 9, 11 and 14 have been amended.

Claims 2-3, 7-8 and 12-13 have been cancelled.

Claims 1, 4-6, 9-11 and 14-15 are pending under consideration.

3. ***Response to Remarks and Amendments***

Applicant's amendments and remarks have been fully and carefully considered.

Independent claims 1, 6 and 11 have been amended to include the new limitation of "**initializing in a generally accessible memory an emulated remote translation table (ERTT) segment**;" and "**mapping the virtual node to a physical node**."

In response to the amendments, a new ground of claim analysis based on previously relied on references (Schimmel, US 6,105,113 and Scott, US Patent Application Publication 2004/0044872) has been embarked. Refer to the corresponding sections of claim analysis for details.

Duty To Disclose Information Material To Patentability

4. The following is a quotation of the appropriate paragraphs of 37 C.F.R. 1.56 that recites Applicants' duty to disclose information material to patentability:

"Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with

respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by § § 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct."

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 4-6, 9-11 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scott (US Patent Application Publication 2004/0044872), and in view of Schimmel (US 6,105,113).

As to claim 1, Scott discloses **a method for translating a virtual memory address into a physical memory address** [Remote Translation Mechanism for a

Multi-Node System (title)] **in a multi-node system** [figure 1 shows a multi-node system; a remote translation mechanism for a multi-node system (abstract)], **the method comprising**:

Initializing [in order for the remote translation mechanism disclosed by Scott to work and function properly, it is inherent that the RTT at all the nodes be initialized and synchronized first before any reference to a memory location resides at a remote node can be served. Without the initialization and synchronization, the RTT may not have the correct information to reach the correct memory location (this also applies to the system disclosed by Schimmel)] **in a generally accessible memory** [figure 5 shows that the RTT comprising a 64K entries memory; figures 6A~6D show the memory organization of the RTT; see below] **an emulated remote translation table (ERTT) segment** [figures 6A~6D show the memory organization of the RTT including the segments (6D); translating the virtual memory address on the remote node into a physical memory address using a remote-translation table (RTT). The RTT contains translation information for an entire virtual memory address space associated with the remote node (abstract)];

providing the virtual memory address at a source node [a remote translation mechanism for a multi-node system. One embodiment of the invention provides a method for remotely translating a virtual memory address into a physical memory address in a multi-node system. The method includes providing the virtual memory address at a source node, determining that the virtual memory address is to be sent to a remote node, sending the virtual memory address to the remote node, and

translating the virtual memory address on the remote node into a physical memory address using a remote-translation table (RTT). The RTT contains translation information for an entire virtual memory address space associated with the remote node (abstract)];

determining that a translation for the virtual memory address does not exist [The method includes providing the virtual memory address at a source node, determining that the virtual memory address is to be sent to a remote node (i.e., does not exist at the local node), sending the virtual memory address to the remote node, and translating the virtual memory address on the remote node into a physical memory address using a remote-translation table (RTT). The RTT contains translation information for an entire virtual memory address space associated with the remote node (abstract); figure 4; paragraph 0006];

determining a virtual node to query based on the virtual memory address [figure 4; paragraph 0031; in one implementation, a local node can identify the virtual node by looking at the VNode field of the virtual address. Checkpoint 404 determines if the virtual node is the same as, or equal to, the local node. If so, flow diagram 400 continues to block 406, wherein the virtual address is translated into a physical address locally using a Translation Look-Aside Buffer (TLB). The local node is then able to address local physical memory space. If the virtual node is not the same as the local node, then flow diagram 400 continues to block 408, wherein the virtual address is translated into a physical address remotely (on a remote node) using a Remote-

Translation Table (RTT). In this fashion, the local node is effectively able to address remote memory space of the remote node (paragraph 0031)];

mapping the virtual node to a physical node [figure 5 illustrates how this mapping is accomplished staring from the Vnode (virtual node) specified by the source node and ending with the corresponding physical address at a local (remote) node];

querying the ERTT segment on the physical node for the translation for the virtual memory address [figure 5 illustrates how this mapping is accomplished staring from the Vnode (virtual node) specified by the source node and ending with the corresponding physical address at a local (remote) node; the corresponding ERTT is the Global Address Space identifier (GASID) and the Remote Translation Table (RTT) as described in paragraph 0019]; **and**

if the translation is received then loading the translation into a translation lookaside buffer (TLB) on the source node [figure 4; paragraph 0019].

Regarding claim 1, Scott does not discuss the details about **how the RTT is managed and whether it is a generally accessible memory**. Note that Applicant defines the term "**generally accessible memory**" as memory that is available for general-purpose use by applications and the kernel [paragraph 0009 of Applicant's disclosure].

However, Scott does teach in figure 5 that the RTT comprising a 64K entries memory and in figures 6A~6D that the memory organization of the RTT.

Further, Schimmel teaches in the invention "System and Method for Maintaining Translation Look-Aside Table (TLB) Consistency" a system and method of maintaining

consistency of a TLB which translates virtual memory addresses into the corresponding physical addresses [abstract]. Particularly, Schimmel teaches that the Page Table Entry (PTE), which is part of the TLB, may be changed by the operating system (i.e., the kernel), and the TLB is updated by the application programs that are responsible for maintaining consistency of the TLB [figure 10; column 12, lines 53-64]. In other words, Schimmel teaches that the TLB is available for general-purpose use by applications and the kernel, therefore it is considered a generally accessible memory.

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicant's invention to recognize that an ERTT is a TBL (i.e., a TBL as far as a local node is concerned, and an ERTT as far as the other remote nodes are concerned) and that a TLB is available for general-purpose use by applications and the kernel, as demonstrated by Schimmel, hence lacking patentable significance.

As to claim 4, Scott teaches that **mapping the virtual node to a physical node uses a mapping provided by an ERTT header located at a well-known location to one or more nodes used by an application** [abstract; figure 5 illustrates how this mapping is accomplished staring from the Vnode (virtual node) specified by the source node and ending with the corresponding physical address at a local (remote) node].

As to claim 5, Scott teaches that **the ERTT header is located on a predetermined virtual node** [figure 5 shows where the ERTT is located with respect to the source node. Since none of the node has all the translation information needed by itself, the collection of all the memories appears to be a predetermined virtual node as far as each of the node is concerned].

As to claim 6, Scott discloses a computerized system for managing virtual address translations, the system comprising:

a plurality of nodes [figure 1 shows a multi-node system] **available for executing programs** [figure 4 shows the computer programs], **each of said nodes having a node memory** [figure 1]; **and**

an operating system [it is common knowledge that all computers and processors are equipped with an operating system; the OS must never create a partition (via the BaseNode and NodeLimit values) that exceeds the number of nodes in the machine (paragraph 0033)] **executable by a source node of the plurality of nodes, the operating system operable to**:

receive a virtual memory address at the source node [abstract; figure 5];

determining that a translation for the virtual memory address does not exist [The method includes providing the virtual memory address at a source node, determining that the virtual memory address is to be sent to a remote node (i.e., does not exist at the local node), sending the virtual memory address to the remote node, and translating the virtual memory address on the remote node into a physical memory address using a remote-translation table (RTT). The RTT contains translation information for an entire virtual memory address space associated with the remote node (abstract); figure 4; paragraph 0006];

determining a virtual node to query based on the virtual memory address [figure 4; paragraph 0031; in one implementation, a local node can identify the virtual node by looking at the VNode field of the virtual address. Checkpoint 404 determines if the

virtual node is the same as, or equal to, the local node. If so, flow diagram 400 continues to block 406, wherein the virtual address is translated into a physical address locally using a Translation Look-Aside Buffer (TLB). The local node is then able to address local physical memory space. If the virtual node is not the same as the local node, then flow diagram 400 continues to block 408, wherein the virtual address is translated into a physical address remotely (on a remote node) using a Remote-Translation Table (RTT). In this fashion, the local node is effectively able to address remote memory space of the remote node (paragraph 0031)];

mapping the virtual node to a physical node [figure 5 illustrates how this mapping is accomplished staring from the Vnode (virtual node) specified by the source node and ending with the corresponding physical address at a local (remote) node];

querying the ERTT segment in the generally accessible memory [refer to "As to claim 1"] **on the physical node for the translation for the virtual memory address** [figure 5 illustrates how this mapping is accomplished staring from the Vnode (virtual node) specified by the source node and ending with the corresponding physical address at a local (remote) node; the corresponding ERTT is the Global Address Space identifier (GASID) and the Remote Translation Table (RTT) as described in paragraph 0019]; **and**

if the translation is received then loading the translation into a translation lookaside buffer (TLB) on the source node [figure 4; paragraph 0019].

As to claim 9, refer to "As to claim 4."

As to claim 10, refer to "As to claim 5."

As to claim 11, refer to "As to claim 1" and "As to claim 6."

As to claim 14, refer to "As to claim 4."

As to claim 15, refer to "As to claim 5."

7. ***Related Prior Art***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Scott et al. (US 6,925,547), "Remote Address Translation in a Multiprocessor System."
- Deneau, (US 6,684,305), "Multiprocessor System Implementing Virtual Memory Using a Shared Memory, and a Page Replacement Method for Maintaining Paged memory Coherence."
- Frank et al., (US 6,490,671), "System for Efficiently Maintaining Translation Lookaside Buffer Consistency in a Multi-Threaded, Multi-Processor Virtual Memory System."
- Hansen, (US 6,101,590), "Virtual Memory System with Local and Global Virtual Address Translation."

Conclusion

8. Claims 1, 4-6, 9-11 and 14-15 are rejected as explained above.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

March 14, 2006

PIERRE BATAILLE
PRIMARY EXAMINER
3/15/06